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Asynchronous Sampling Rate Conversions in Digital Communications Systems

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Abstract—The problem of resampling digital signals at an output sampling rate that is incommensurate with the input sampling rate is the topic of this paper. This problem is often encountered in practice, as for example in the multiplexing of video signals from different sources for the purpose of distribution. There are basically two approaches to resample the signals. Both approaches are thoroughly described and practical circuits for hardware implementation are provided. A comparison of the two circuits presented in the paper shows that one circuit requires a division to compute the new sampling times. This time scaling operation adds complexity to the implementation with no performance advantage over the other circuit, and makes the "division free" circuit the preferred one for resampling.

Keywords—Asynchronous resampling, sampling rate conversion, cable modem, interpolation, phase locked loop.

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1 Introduction

Today’s TV networks offer a variety of programs such as news, sport, movies or TV shows. The broadcasting of different video sources over the same network is made possible by gathering the content from the sources at a main distribution center called the headend. The programs may be delivered to the headend over a cable feed or satellite link or may be played from a magnetic tape or optical disk [1].

At the headend the incoming signals are received and processed for transmissions over the distribution network. The nature of the system calls for a sampling rate conversion of the received signals. The reason is that the incoming signals, normally Quadrature Amplitude Modulation (QAM) signals, are received at different sampling rates, and the processing which combines the QAM signals for transmissions over the network requires that all signals be at the same sampling rate.

The incoming QAM signals originate from different transmitters, and thus have different data rates. The pulse shaping filter in the receiver, which normally has a square-root raised cosine frequency response, is designed to run at an integer multiple of the rate at which the data is received, i.e., the input data rate. The sampling rate of the incoming signal, referred to in the sequel as the input sampling rate, is then an integer multiple of the input data rate. The received signals must then be resampled at a common sampling rate, i.e., the output sampling rate, so they can be combined together, and transmitted over the distribution network.

The problem of sampling rate conversion is illustrated in Figure 1, which shows N incoming signals, denoted by \( x_1[m_1], x_2[m_2], \ldots, x_N[m_N] \), and their respective input sampling clocks denoted by \( clk_{in_1}, clk_{in_2}, \ldots, clk_{in_N} \) with the sampling rates \( F_{in_1}, F_{in_2}, \ldots, F_{in_N} \). The sampling rate converter resamples the input signals at the sampling rate \( F_{out} \). The output signals \( y_1[k], y_2[k], \ldots, y_N[k] \) are then combined to produce \( z[k] \), which is then passed to a digital to analog converter (DAC) to produce \( z(t) \).

The block of interest in this paper is the sampling rate converter. Resampling the QAM signals at an output sampling rate that is incommensurate with the input sampling rates is not straightforward. There are basically two approaches to this problem. One approach takes the input sampling rate as a reference to control the digital resampling. The other method uses the output sampling rate as the reference. The thrust of this paper is to describe and provide circuits for both methods. It is shown that one method leads to less circuit complexities with no performance loss.

The asynchronous resampling of digital signals is far from being a new topic, however, to the best of the authors’ knowledge, the subtle differences between the two methods of resampling have not been reported in the open literature. As sampling rate conversion is of paramount importance in digital systems, it is believed there is interest in presenting both methods in parallel, highlight their differences, and provide practical circuits for hardware implementation.
The paper is organized as follows. After briefly reviewing the theory of resampling in Section 2, the operations of resampling in hardware is described in Section 3. Circuits for both methods are provided in Section 4. Verification of the circuit operations is the object of Section 5. Conclusions are given in Section 6.

2 Principle of Resampling

Resampling consists of taking a sequence of samples, \( x[m] \equiv x(mT_{\text{in}}) \), at sampling rate, \( F_{\text{in}} = 1/T_{\text{in}} \), and generating a new sequence, \( y[k] \equiv y(kT_{\text{out}}) \) by means of interpolation between the samples of \( x[m] \), as described by the block diagram in Figure 2. Inside the resampler shown in Figure 2 there is an interpolator whose purpose is to interpolate between the input samples to produce the output interpolants. By interpolants, it is understood the samples \( y[k] \). In this section, the mathematical model for digital interpolation given in [2], [3] is reviewed.

To resample at \( F_{\text{out}} = 1/T_{\text{out}} \), the interpolants are computed at times \( kT_{\text{out}} = (m_k + \mu_k)T_{\text{in}} \) using \( I_2 - I_1 + 1 \) input samples, \( x[m_k - I_1], x[m_k - I_1 + 1], \ldots, x[m_k - I_2] \) as follows:

\[
y(kT_{\text{out}}) = \sum_{i=I_1}^{I_2} x[(m_k - i)T_{\text{in}}]h_1(i + \mu_k)T_{\text{in}}]
\]

where \( m_k = \text{int}[kT_{\text{out}}/T_{\text{in}}] \) is the basepoint index, \( \mu_k = kT_{\text{out}}/T_{\text{in}} - m_k \) is the fractional interval, \( h_1(t) \) is the interpolating function, and \( \text{int}[\cdot] \) is the integer part of a real number.

The simplest interpolator is the linear interpolator. It only uses 2 samples (i.e., \( I_1 = -1, I_2 = 0 \)) and the interpolating equation (1) reduces to

\[
y[k] = x[m_k](1 - \mu_k) + x[m_k + 1]\mu_k
\]

where \( T_{\text{in}} \) has been set to 1 with no loss of generality. The computation of \( y[k] \) using (2) is illustrated in Figure 3. Clearly, \( y[k] \) is the point on the line passing through \( x[m_k] \) and \( x[m_k + 1] \) at a distance of \( \mu_k \) from \( x[m_k] \).

Equation (2) is implemented in hardware with a 2-tap filter as shown in Figure 4, where the blocks labeled “reg” are registers holding the input samples used in the interpolation.

3 Operations of Resampling

3.1 Resampling Operations in Hardware

The key operation of a resampler is the generation of the basepoint index \( m_k \) and fractional intervals \( \mu_k \). This part presents the hardware circuitry required to generate \( m_k \) and \( \mu_k \). These circuits are the essential blocks in asynchronous resampling rate converter.

Basically, two time base generators are needed to compute the sampling times, \( kT_{\text{out}} \). One generator is clocked by the input clock at frequency, \( F_{\text{in}} \) (units of samples/second) and the other generator is clocked by
slopes can be made equal by modifying the step size of one of the time base generators by an appropriate amount. The right amount is estimated by means of a phase lock loop (PLL). In other words, the PLL can either estimate $\hat{F}_\text{in}$ or $F_\text{out}$ so that $\hat{F}_\text{in}/F_\text{in} = F_\text{out}/T_\text{out}$ after the PLL has converged. The timing offset, $\Delta Y$, is removed in the process of finding the right step size.

There are two ways to establish synchronization. Either $Y_\text{out}$ is taken as the reference to estimate $\hat{Y}_\text{in}$, or $Y_\text{in}$ serves as the reference to estimate $\hat{Y}_\text{out}$. In this paper, circuits are given for both methods in Section IV. The sampling rate converter circuit which uses the output ramp as the reference is referred to as “a resampler with input clock time base”. The circuit which uses the input ramp as the reference is referred to as “a resampler with output clock time base”.

4 Circuit Description

4.1 Resampler with Input Clock Time Base

The output ramp, $Y_\text{out}$ is the reference to construct the ramp, $Y_\text{in}$ which in this method is then used to compute $m_\text{k}$ and $\mu_\text{c}$. The PLL is set up as follows.

Output ramp $Y_\text{out}$ is normalized by fixing the input of the accumulator (i.e., step size) in Figure 5 to $T_\text{out} = 1$. This causes the output, $Y_\text{out}$, to be scaled by $1/T_\text{out}$. Note that by normalizing the output the circuit no longer needs $\hat{T}_\text{out}$. As shown in Figure 7, in the process of normalizing the output clock time base generator, the output of the input clock time base generator gets normalized by $T_\text{out}$. Its input, denoted by $\hat{T}_\text{in}/T_\text{out}$, is the estimate produced by the PLL to synchronize input and output time bases.

A block diagram of the resampler with input clock time base is shown in Figure 8. It has three inputs, $x[n]$, $\text{clk}_\text{in}$ and $\text{clk}_\text{out}$ and one output, $y[k]$. $N$ copies of this circuit are required to process $N$ input signals, as illustrated in Figure 1. In Figure 8 a clock at frequency $F_c = MF_\text{in}$ is synthesized from $\text{clk}_\text{in}$ using a built-in PLL in the FPGA. $M$ must be chosen large enough so $F_c > F_\text{out}$. The block labeled “Output clock time base” in Figure 8 is the time base generator shown in Figure 5, where the input has been set to 1 (normalization by $T_\text{out}$). The block labeled “Input clock time base” is the circuit in Figure 7 where the input clock is at frequency $F_c = MF_\text{in}$. Its input, denoted by step adjustment in
The presence of different clocks inside the circuit in Figure 8 calls for a special structure, which allows samples to be written and read using different physical clocks. The average writing and reading rates are the same but the access to the samples inside the structure, represented by the block labeled “Clock domain interface” in Figure 8, occurs at different instants of time. Such a structure is implemented with a circular buffer and logic to control the access of the buffer. Two of these blocks are needed, one to interface the clocking of the input samples and the interpolator and the other one to interface the output of the interpolator and the clocking of the output samples.

The last block which remains to be described in Figure 8 is the “Basepoint index and fractional interval generator” block. This module uses the reconstructed input ramp, \( \frac{Y_{in}}{T_{out}} \), to produce \( m_k \) and \( \mu_k \). A new pair of values for \( m_k \) and \( \mu_k \) is computed at a positive clock edge of \( F_c \) every time the integer part of \( \frac{Y_{in}}{T_{out}} \) increases by 1. We say that \( \frac{Y_{in}}{T_{out}} \) has crossed an integer number and an integer cross-over was detected. An output interpolant is generated by computing its basepoint index \( m_k \) and fractional interval \( \mu_k \) as follows.

In the case of the linear interpolator, \( m_k + 1 \) is the index of the last received sample and \( m_k \) is the index of the previous received sample, as shown in Figure 4. The new interpolants are generated at positive edges of \( F_c \).

Most of the time, especially if \( M \) is large, this clock edge does not coincide with a positive clock edge of \( clk_{in} \). The situation with \( M = 4 \) is depicted in Figure 11,
Figure 10: Resampler with output clock time base.

Figure 11: Timing relation in input clock time base resampling.

where the top graph shows the position of $y[k]$ with respect to the input samples and the bottom graph shows all three clocks.

The computation for $\mu_k$ depends on which clock edge of $F_c$ the integer cross-over was detected. Since $F_c$ is $M$ times faster than $F_{in}$, $M$ clock cycles of $F_c$ occur between clock cycles of $F_{in}$. Suppose that between input sampling times $mT_{in}$ and $(m+1)T_{in}$, an integer cross-over is detected at the $i^{th}$ positive clock edge of $F_c$. Then $\mu_k$ is given by

$$\mu_k = \frac{l_k}{M} - \frac{T_{out}}{T_{in}} \times \frac{Y_{in}}{T_{out}}.$$  \hspace{1cm} (6)

In Figure 11, we show the case for $M = 4$, $l_k = 1$, $l_k+1 = 3$.

There is a division in (6) which needs explanation, as it is not required in the second circuit, and causes additional complexity in the calculation of $\mu_k$. The fractional part, $\frac{Y_{in}}{T_{in}}$, which is used to compute the time that separates the new interpolant from the input sample, is expressed as a fraction of the output clock cycle. This time must be converted in units of fraction of the input clock cycle to yield $\mu_k$. This is achieved in (6) by dividing $\frac{Y_{in}}{T_{out}}$ by $\frac{T_{in}}{T_{out}}$.

4.2 Resampling with Output Clock Time Base

In this method, $Y_{in}$ is used as the reference to construct $Y_{out}$, which is then used to compute $m_k$ and $\mu_k$. The circuit is shown in Figure 10. Similarly the clock, $clk$, at frequency $F_c = M \times F_{out}$ is synthesized. Typically, $M$ will be small, even equal to 1 in which case no PLL-synthesizer is needed, since the output sampling rate is normally much higher than the input rates. In this circuit, the step size of the “Input clock time base” block is set to 1 and the step size of the output clock time base is determined with the PLL. The main difference is that a new interpolant is produced at every positive edge of the resampling clock $F_{out}$. In this case, whenever an integer cross-over in the reconstructed output ramp is detected, a new input sample is loaded into the interpolator. The fractional interval is simply given by

$$\mu_k = \frac{Y_{out}}{T_{in}}.$$  \hspace{1cm} (7)

In this case there is no division since the fractional part is already expressed as a fraction of the input clock cycle. Recall that in this method the step size of the output clock time base generator is adjusted to reproduce the ramp of the input clock, and therefore its content is directly given in the input clock domain.
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The timing relation for the case $F_c = 2F_{\text{out}}$ is depicted in Figure 12.

As internal PLL synthesizers are readily available in FPGA, any of the two methods can be applied independently on the relation between input and output sampling rates. Since the second circuit leads to less hardware complexity by avoiding a division, the second method, namely resampling with output clock time base, is much preferred.

5 Verification

Both resampler circuits were simulated in Matlab/Simulink software. The input signal $x[m]$ was generated with 4 samples per symbol using a random BPSK sequence and a raised cosine pulse shaping filter with a roll-off factor equal to 0.25.

The first simulation is set up as follows. A resampler with input clock time base is simulated using the Simulink software to resample the input signal from input rate $F_{\text{in}}$ to output rate $F_{\text{out}} = (4/3)F_{\text{in}}$. The circuit is clocked by system clock $clk$ at rate $F_c = 4F_{\text{in}}$ (i.e., $M = 4$). The PLL (see Figure 9) was set up with small loop gains to reduce the effect of timing jitter, which is the random fluctuation in the timing [5].

The second simulation is set up to show the Power Spectral Densities (PSDs) of the resampled signals. The PSDs of the resampled signals were estimated using to 1 second. Figure 16 shows the two ramps which are synchronized after the step size has been converged.

Figure 17 shows sets of input samples (marked with a circle) and output interpolants (marked with an asterisk) after the circuit has found the correct step size and the two time bases have synchronized. The corresponding fractional intervals (marked with an asterisk) are shown in Figure 18. Cubic interpolator is used in this simulation.

The second simulation is set up to show the Power Spectral Densities (PSDs) of the resampled signals. The PSDs of the resampled signals were estimated using...
Theoretical curves (dashed curves) are also plotted in Figure 21 and Figure 22 (solid curve). For conversion rate \( \approx 0.59 \).

The roll-off factor \( \mu \) is chosen to be 0.59 of the input rate, where \( T \) being the symbol period and \( |\beta|T \) is the excess bandwidth of the filter. The excess bandwidth is the bandwidth occupied beyond the Nyquist bandwidth of \( 1/T \).

\[
H(f) = \begin{cases} 
1, & \text{if } |f| \leq \frac{1-\beta}{2T} \\
\frac{1}{2} \left[ 1 + \cos \left( \frac{\pi T}{\beta} \left[ |f| - \frac{1-\beta}{2T} \right] \right) \right], & \frac{1-\beta}{2T} < |f| \leq \frac{1+\beta}{2T} \\
0, & \text{otherwise.}
\end{cases}
\] (8)

In Equation (8), \( T \) is the symbol period and \( \beta \) is the roll-off factor, which is a real number between 0 and 1. The roll-off factor \( \beta \) determines the excess bandwidth of the filter. The excess bandwidth is the bandwidth occupied beyond the Nyquist bandwidth of \( 1/(2T) \).

The close agreement between the experimental and theoretical curves strongly suggests that the circuits work properly. From the plots, the performances of both circuits appear to be identical. However, the resampler using output clock time base requires no division for the computation of \( \mu_k \) and therefore is the preferred one.

6 Conclusion

Two resampler circuits were described and simulated in the Matlab/Simulink software. Simulations show that both circuits offer similar performances but one of them, namely the resampler circuit which uses the output clock time base has a hardware implementation advantage over the other one. It does not require any division to compute the position of the new samples with respect to the incoming samples. This is a significant advantage in FPGA implementation.
REFERENCES


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