

Provided for non-commercial research and educational use only.
Not for reproduction or distribution or commercial use.



This article was originally published in a journal published by Elsevier, and the attached copy is provided by Elsevier for the author's benefit and for the benefit of the author's institution, for non-commercial research and educational use including without limitation use in instruction at your institution, sending it to specific colleagues that you know, and providing a copy to your institution's administrator.

All other uses, reproduction and distribution, including without limitation commercial reprints, selling or licensing copies or access, or posting on open internet sites, your personal or institution's website or repository, are prohibited. For exceptions, permission may be sought for such use through Elsevier's permissions site at:

<http://www.elsevier.com/locate/permissionusematerial>



ELSEVIER

Microelectronics Journal 38 (2007) 67–75

Microelectronics
Journal

www.elsevier.com/locate/mejo

Recent advances in modeling the underfill process in flip-chip packaging

J.W. Wan^a, W.J. Zhang^{b,*}, D.J. Bergstrom^b

^aGuangzhou University, China

^bDepartment of Mechanical Engineering, University of Saskatchewan, 57 Campus Dr., Saskatoon, Sask., Canada S7N 5A9

Received 21 July 2006; accepted 25 September 2006

Available online 27 November 2006

Abstract

Flip-chip underfill process is a very important step in the flip-chip packaging technology because of its great impact on the reliability of the electronic devices. In this technology, underfill is used to redistribute the thermo-mechanical stress generated from the mismatch of the coefficient of thermal expansion between silicon die and organic substrate for increasing the reliability of flip-chip packaging. In this article, the models which have been used to describe the properties of underfill flow driven by capillary action are discussed. The models included apply to Newtonian and non-Newtonian behavior with and without the solder bump resistance for the purpose of understanding the behavior of underfill flow in flip-chip packaging.

© 2006 Elsevier Ltd. All rights reserved.

Keywords: Model; Underfill flow; Flip-chip packaging

1. Introduction

Faster, smaller, and cheaper components have been regarded as the future trend in electronic appliances, e.g., laptop personal computers, cell phones, etc. [1]. This trend has set more stringent requirements on the packaging technology in the electronics industry. One of the most promising packaging methods today is the flip-chip technology because it offers superior electrical performance due to the shorter electrical connections between the chip and substrate and very high input/output capacity and the smallest possible package size.

Flip-chip packaging is a first-level interconnect technology and was first developed about 40 years ago. Since its invention, great efforts have been devoted to the research and development of this packaging technology. One of the most successful flip-chip packaging processes is the controlled collapse chip connection (C4) invented by IBM in 1960s, in which solder bumps are used to electrically couple the silicon ICs to the substrate. In C4 flip-chip package (Fig. 1), the solder bumps are 100–250 μm in diameter and 50–200 μm high [2].

Before the past decade, however, research and development of the flip-chip technology have not been aggressive because wire bonding technology met the needs of the packaging industry. In the wire bonding technology shown in Fig. 2, the interconnection between the die and the substrate is made using a wire. The die is attached to the substrate with the active face up. A wire is bonded first to the active surface of the die, then looped and bonded to the substrate. The process is performed by high-speed machines that can bond several wires per second. But as the industry calls for smaller and higher input/output capacity integrated circuit (IC), more wires are needed. As chip size decreases and the number of input/output (I/O) increases, pads and wires are moved more closely together, making it more difficult and expensive to build the equipment needed to produce ICs. The closer together the wires at the periphery of the die, the more technical issues arise because the wires have to be bonded along the die's periphery. Additionally, when wires are bonded more closely together, electromagnetic interference caused by them becomes a significant problem. Therefore, it becomes difficult for the wire bonding technology to further increase I/O capacity and to reduce the packaging size.

The flip-chip technology solves this challenge by making the die connected to the substrate via a conductive “bump”

*Corresponding author. Tel.: +1 306 9665 478; fax: +1 306 9665 427.
E-mail address: chris.zhang@usask.ca (W.J. Zhang).

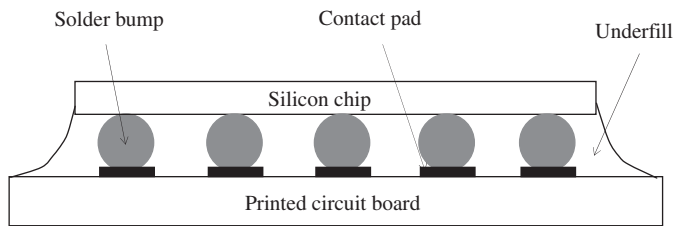


Fig. 1. Illustration of C4 flip-chip packaging.

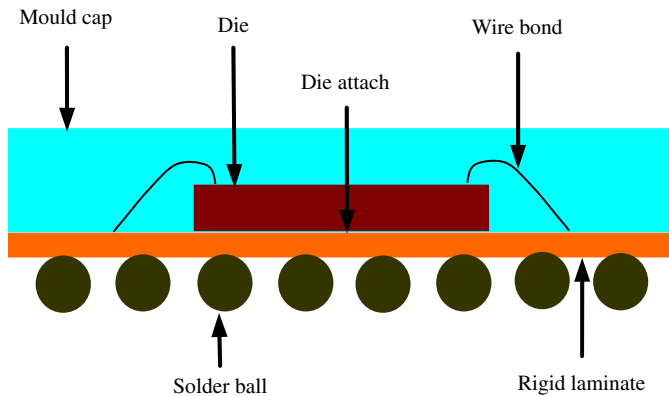


Fig. 2. Wire bond CABGA cross-section.

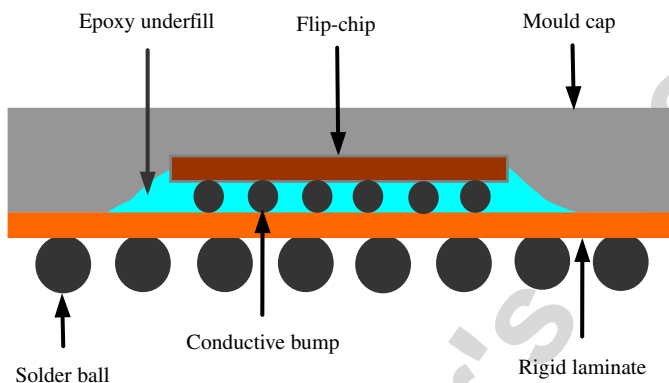


Fig. 3. Flip-chip CABGA cross-section.

[3]. In particular, the active face of the die is attached to the bump which is then attached to the substrate. The bumped die is "flipped over" the substrate (Fig. 3). Therefore, flip-chip package has the advantages of high I/O density capability, improved electrical performance due to the short interconnect from chip to substrate, reduced size and weight, and improved thermal performance since the top surface of the chip can be used for an efficient cooling component to deal with the increasing power density required by the trend toward the devices using higher packaging densities.

The major challenge with flip-chip packaging technology originates from thermal mechanical stresses caused by the mismatch of the coefficients of thermal expansion between the silicon chip and the cost-effective organic substrate. This is because all materials undergo some dimensional

change when their temperatures change. Most materials expand when heated because increased thermal energy causes atomic or molecular distances to increase. The parameter used to quantify the dimensional–temperature relationship is the coefficient of thermal expansion (CTE). The difference in CTE between the silicon chip and the organic substrate can cause significant thermal stresses on interconnects during temperature cycling and ultimately results in fatigue cracking and electrical failure.

To solve the CTE mismatch problem resulting from assembling the flip-chip with a polymer-based organic substrate, the simplest and most cost-effective approach is to fill the gap between the chip and the organic substrate with an appropriate composite to transfer the thermal–mechanical stress away from the fragile bump zone to a more strain-tolerant region [4–11]. The underfill is an encapsulant, which is coated over the active area of the die and the interconnect structure. The underfill serves at least two purposes: (1) performance enhancement, and (2) chip/joint protection. It should be noted that the underfill movement is constrained by the very rigid and low expansion chip in its plane. The underfill will expand in the vertical direction with its own CTE. Therefore, underfill should have a CTE value that approximates the value of the solder bump to avoid the mismatch of the CTE between underfill and the solder joint in the vertical direction.

2. Flip-chip encapsulation technology

Flip-chip encapsulation technology can be classified into conventional underfill, no-flow underfill, and injection underfill (molded underfill).

Conventional underfill technology has been developed and practiced for nearly 20 years. At present, more than 90% of the underfill processes employed in industry are realized by dispensing liquid encapsulant at elevated temperatures along the periphery of one or two sides of the chip and allowing capillary action to draw the encapsulant into the micro-cavity [2]. During the underfill processes, the capillary action (i.e., surface tension) draws the encapsulant into the cavity between the chip and the substrate. After the filling is completed, the chip and substrate assembly is taken to an oven where the underfill is cured. Since the filling process is based on capillary action, the filling process is slow. This situation becomes significant with an increase of chip size and fine bump pitch.

The no-flow underfill process was first reported by Wong and Baldwin [12]. Compared with the conventional underfill process (see Fig. 4), the no-flow underfill process has potential advantages over the conventional underfill process due to its simplicity. As the no-flow underfill process eliminates the strict limits on the viscosity of underfill encapsulant and the package size, and simplifies the conventional underfill process by combining solder reflow and underfill cure into one step, it can improve the production efficiency. However, since the pre-deposited

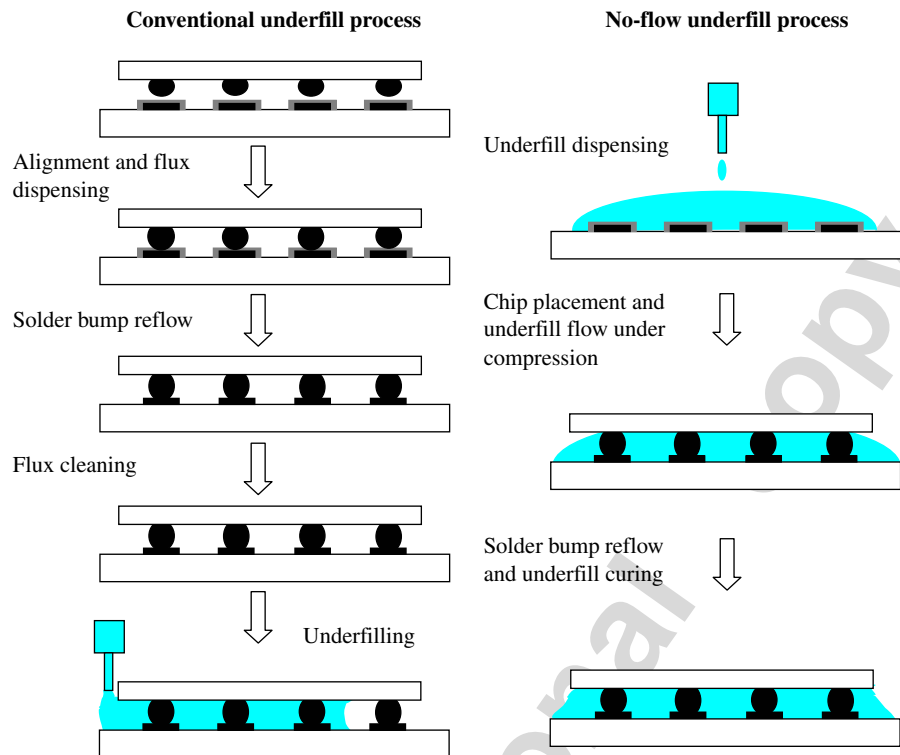


Fig. 4. Conventional underfill processes vs. no-flow underfill process.

underfill cannot contain high levels of silica filler due to the interference of the filler with solder joint formation, the high CTE of the underfill results in the poor reliability of the package [13]. Also, the placement of the chip requires more accuracy. Since no-flow underfill process is difficult to control during the compression flow of the encapsulant material, void formation is often observed in many flip-chip no-flow underfill packages [13]. Voids in the underfill, especially voids near the solder bumps, may cause early failure due to stress concentration, underfill delamination, and solder extrusion. Currently, no-flow underfill is mainly applied for the low I/O and small-size products for which reliability is of less concern.

Another way to make underfill fluid flow fast is to use injection filling [14–17] that introduced the use of a vacuum to increase the driving force. The vacuum method enables shorter filling times than those required by the dispensing process, but the maximum driving force is limited to the atmospheric pressure. The major concerns on the vacuum molded underfill technology are the compound flush in the air vent area and the uncompleted fill. An insufficient mold vacuum (90–95%) will also cause the uncompleted fill issue within the chip area [16]. When the underfill material is not uniformly distributed or there are voids in the underfill region, there will be a reliability issue in the function of the packaged chip. Han and Wang [15] reported a pressurized underfill encapsulation method. Their method injects the encapsulant under high pressure into the mold which surrounds and seals the chip. In this case, the flow is generated by the pressure exerted from the inlet rather than

by the surface tension at the flow-front. The underfill process can be done at either constant pressure or constant flow rate. This method can significantly reduce filling time compared to that required by the dispensing process, since the fast-curing underfill materials can be used and the filling can be done at room temperature. The main problem existing in the injection filling method is that the flip-chip geometry has a higher resistance to the mold flow which results in the phenomenon that the air is trapped under the chip. The study reported by Rector et al. [18] showed that the voids were observed in the molded underfill packages using an acoustic microscope. The poor reliability caused by the air void which accompanies in the injection process and the complexity generated in the injection mold are the main challenges for the application of injection underfill technology.

3. Analytical modeling of the underfill flow process

Although the conventional underfill has been developed and practiced for nearly 20 years, it still prevails in industrial practice due to its high reliability, especially with the development of fast-flow, fast-cure underfill materials obtained in recent years. Currently, typical underfill takes less than 40 s to underfill a common-size chip (6 mm × 6 mm) and a few minutes for curing in a typical industry setting. Therefore, in conventional underfill the prediction of the underfill flow characteristics in a flip-chip package driven by capillary action is very important for

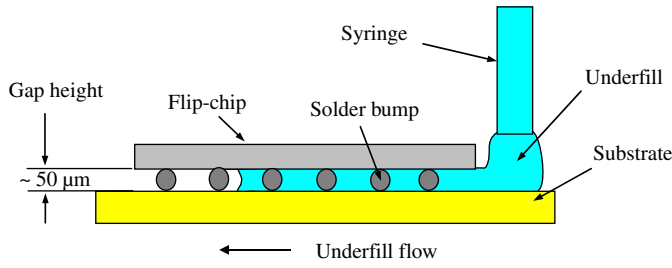


Fig. 5. Dispensing underfill flow process.

controlling the filling process and optimizing the design of the flip-chip package.

Fig. 5 is a schematic diagram of underfill flow process. The encapsulant is dispensed along the periphery of one side of the chip and drawn by capillary action through the micro-cavity between the chip and the substrate. The typical gap height is around 50 μm, and solder pitch is 200–500 μm. In order to reduce the viscosity and to make the fluid flow more quickly, the liquid encapsulant is usually heated up to 80–90 °C.

3.1. Modeling underfill flow process with the Washburn model

The underfill flow process is usually evaluated by three performance indices: (1) the fluid filling time, (2) the flow front position as shown in Fig. 6, and (3) the fluid distribution. A model describing the first two indices is needed for process design optimization and control. Most studies reported in the literature [19–25] applied the Washburn model [26] to the underfill flow analysis in the case of two parallel plates. In the Washburn model, it was assumed that the flow is laminar, one-dimensional, incompressible, and fully developed flow of a Newtonian fluid. This results in the following expression for the location of the flow front

$$x_f^2 = \frac{\sigma h \cos \theta}{3\mu} t, \quad (1)$$

where σ is the surface tension coefficient, x_f is the position of the flow-front at time t , θ is the contact angle, μ is the viscosity of the Newtonian fluid, and h is the thickness of the cavity (see Fig. 1.8). From Eq. (1), the fluid filling time t_f for a cavity is

$$t_f = \frac{3\mu L^2}{\sigma h \cos \theta}, \quad (2)$$

where L is the length of the cavity.

Although the Washburn model has been widely used in the underfill flow analysis in flip-chip packaging, unfortunately, the filling time calculated with this model does not agree well with the observation measured in the underfill flow of a flip-chip packaging [24,27–30]. One reason for this is that the Washburn model was developed for a Newtonian fluid, while underfill materials for flip-chip packaging typically exhibit non-Newtonian behavior

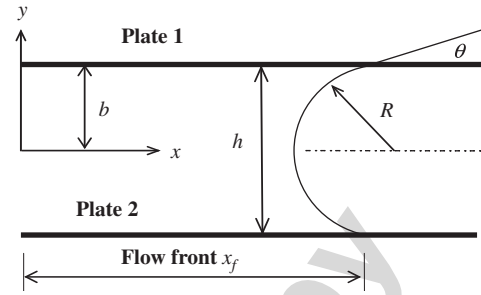


Fig. 6. Underfill flow between two parallel plates.

[24,28]. Another reason is that the Washburn model was originally developed for the capillary flow in a cylindrical tube and did not consider the influence of the solder bump resistance on the underfill flow in flip-chip packaging.

3.2. Improved Washburn models

Based on Washburn model, Han and Wang [24] developed a method that incorporates the concept of a “dynamic contact angle.” The dynamic contact angle concept proposed by Schonhorn et al. [31] describes the change of the contact angle with time for an open-flow process of polymer melts from the initial state to an equilibrium state. Newman [32] first used this concept for the capillary flow in a circular tube and used the following equation to describe the contact angle:

$$\cos \theta = \cos \theta_e (1 - ae^{-ct}), \quad (3)$$

where a and c are coefficients, determined by

$$a = 1 - \frac{\cos \theta_0}{\cos \theta_e} \quad (4)$$

and

$$c = \frac{\sigma}{\eta M}, \quad (5)$$

where θ_0 is the initial contact angle, θ_e is the contact angle at an equilibrium state, M is a constant which depends on the surface in contact with the encapsulant, and η is the viscosity of non-Newtonian fluid.

Employing Eqs. (3)–(5) and the Washburn model, Han and Wang obtained the following equation for the capillary flow between two parallel plates, which is similar to an equation developed by Newman [32] for a capillary flow in tube

$$t_f = \frac{3\eta L^2}{\sigma h \cos \theta_e} + \frac{a}{c} (1 - e^{-ct_f}), \quad (6)$$

since Eq. (6) is a nonlinear function of filling time t_f , his model needs to be solved using an iterative method and does not give a closed-form solution.

Han and Wang [24] experimentally tested this model for a flip-chip underfill flow. The comparison between the experimental and predicted results is given in Table 1. The experimental conditions for the results in Table 1 were the

Table 1
Measured and theoretical filling times

Temperature (°C)	80	50	23	23	23
Fraction of volume filled (%)	0.926	0.676	0.25	0.402	0.646
Measured filling time (s) (Han and Wang, 1997a)	60	180	180	600	2700
Filling time calculated with Washburn model (s) (Eq. (2))	8.58	17.6	9.84	27.35	77.47
Filling time calculated with Han-Wang model (s) (Eq. (6))	46.6	133.6	121.4	330.0	835.1
Filling time calculated with the proposed analytical model (s) (Eq. (8))	61.5	189.5	187.7	535.4	1502

length of the chip was 7 mm, the thickness of the cavity was 100 μm, the solder pitch was 250 μm, the clearance between adjacent solder joints was 90 μm, the initial contact angle $\theta_0 = 84.8^\circ$, and $M = 17.1$.

From Table 1, it is noted that the improved Washburn model is superior to the original Washburn model for predicting the underfill process in a flip-chip package. However, the predicted filling times with the improved Washburn model still did not match the experimental results. There are two possible reasons for this discrepancy. First, the viscosity in this model is for a Newtonian fluid. However, the underfill material itself is a non-Newtonian fluid, thus this model may not be applicable to the underfill flow in flip-chip packaging. Second, this model was developed for the underfill flow between two parallel plates. Therefore, it did not include the effect of the solder bump on the underfill flow.

In regard to the problems existed in Han–Wang model, Wan et al. [33] proposed a new analytical model, in which the effect of the solder bump on the underfill flow was included. In this model, the flow front and filling time are expressed, respectively, as

$$x_f^2 = \frac{4b^2 \sigma \cos \theta_e (W^2 + hW + dW - dh)}{3\mu h W (W + d)} \left[t + \frac{a}{c} (e^{-ct} - 1) \right], \quad (7)$$

$$t_f = \frac{3\mu W (W + d)}{h \sigma \cos \theta_e (W^2 + hW + dW - dh)} x^2 + \frac{a}{c} (1 - e^{-ct_f}). \quad (8)$$

This model is also a nonlinear function of filling time t_f and calls for an iterative procedure. The filling time calculated from this analytical model was compared with the measured filling time, as well as predictions using the Washburn and Han–Wang models (respectively), as shown in Table 1. From the results, it can be seen that the prediction using the proposed analytical model matches the measured filling times better than the predictions using both the Washburn model and the Han–Wang model. This indicates that the flow resistance caused by the solder bump has a significant effect on the underfill flow for the specific conditions of this case. However, all the simulations are in poor agreement with the measured results at 23 °C for volume fractions of 0.402% and 0.646%. In this case, the difference between the experimental and the theoretical results may be caused by the temperature and time

dependence of the viscosity. This is because the underfill flow process is to a certain degree coupled with the fluid curing process. The solidification process will affect the viscosity of the fluid, and such an effect becomes more significant with an increase in the filling time. When the underfill flow is performed at lower temperatures and longer filling times, the viscosity may increase significantly with time.

3.3. Analytical models for viscous non-Newtonian fluid

It can be noted that the above analytical models reported by Han and Wang [24] and Wan et al. [33] are basically generated from the Newtonian fluid assumption. This means that to describe a real flip-chip underfill process, a non-Newtonian fluid analytical model should be employed. In the study reported by Wan et al. [34], the power-law constitutive equation is employed for describing the non-Newtonian fluid behavior in the flip-chip package as the underfills used in flip-chip packaging show the non-Newtonian property of the underfill materials. Based on this constitutive equation, two analytical models with closed-form solutions were derived for predicting the fluid filling time and flow front position. The first model, called Model I, uses the geometry of two parallel plates as an approximation to the flip-chip package, while the second model, called Model II, considers the geometry of two parallel plates within which an array of solder bumps is present. Based on the study, the flow front in flip-chip packaging (Model II) is calculated with the following equation, as a function of filling time:

$$x_f = \frac{h}{2} \left(\frac{2\sigma \cos \theta (W^2 + dW - dh)}{m h W (W + d)} \right)^{(1/n+1)} \left(\frac{n+1}{2n+1} t \right)^{(n/n+1)}, \quad (9)$$

where m and n are coefficient and index of power-law viscosity equation, which are temperature dependent with the units of (Pa·sⁿ) and dimensionless, respectively; W is the clearance between two adjacent solder joints, and d is the solder diameter. Eq. (9) can be rearranged to obtain the following expression for the filling time for a cavity of length x :

$$t_f = \frac{2n+1}{n+1} \left(\frac{m h W (W + d)}{2\sigma \cos \theta (W^2 + dW - dh)} \right)^{1/n} \left(\frac{2x}{h} \right)^{(n+1)/n}. \quad (10)$$

The above analytical model includes Model I (by taking the solder diameter zero) and the Washburn model (by taking the power law index $n = 1$ and solder diameter zero). Therefore, it can not only predict the underfill flow in flip-chip packaging for non-Newtonian fluid and Newtonian fluid, but also can predict the underfill flow between two parallel plates for both non-Newtonian and Newtonian fluid. An experimental investigation showed that this model can give good prediction for current used underfill materials [35].

4. Numerical modeling of underfill flow in flip-chip packaging

An analytical model with closed-form solution as discussed above is very useful for the process control and the parameter analysis, but it can not provide the information of the fluid distribution in two- or three-dimensional geometry. Therefore, it is not suitable for predicting the flow front distribution shape and the position of the air void trapped in the flow process, which are concerned problem for the reliability of flip-chip packaging. To meet these requirements, many numerical studies have been carried out in the literature [2,24,28,35,36].

In the study reported by Nguyen et al. [28], the plastic integrated circuit encapsulation computer aided design (PLICE-CAD) simulation code was developed for calculating the filling time and for simulating the flow front distribution in flip-chip packaging. In their study, the predicted motion of the flow front was slower than that of the observed front. They did not provide an explanation for this discrepancy. Besides, the authors treated a non-Newtonian encapsulant as Newtonian fluid.

In the study reported by Han and Wang [24], the Hele–Shaw approximation was used to describe the underfill flow characteristics for the encapsulant material FP4510. The Hershel–Bulkey model was used to describe the non-Newtonian behavior of the underfill material. Hele–Shaw approximation was generally used to describe the underfill flow characteristics [24]. Under these assumptions, the govern equations are given by

$$\frac{\partial \rho}{\partial t} + \frac{\partial(\rho u)}{\partial x} + \frac{\partial(\rho v)}{\partial y} + \frac{\partial(\rho w)}{\partial z} = 0, \quad (11)$$

$$0 = \frac{\partial}{\partial z} \left(\eta \frac{\partial u}{\partial z} \right) - \frac{\partial p}{\partial x}, \quad (12)$$

$$0 = \frac{\partial}{\partial z} \left(\eta \frac{\partial v}{\partial z} \right) - \frac{\partial p}{\partial y}, \quad (13)$$

$$\rho c_p \left(\frac{\partial T}{\partial t} + u \frac{\partial T}{\partial x} + v \frac{\partial T}{\partial y} \right) = \frac{\partial}{\partial z} \left(k \frac{\partial T}{\partial z} \right) + \eta \dot{\gamma}^2 + \frac{d\alpha}{dt} H, \quad (14)$$

where u , v , and w are the velocity components in the x , y , and z directions, respectively, p is the pressure, T is the

temperature, α is the degree of cure, and H is the heat generation due to curing. Eq. (9) is continuity equation, Eqs. (10) and (11) are the momentum equations in the x and y direction, Eq. (12) is energy equation. For a capillary driven flow, the boundary conditions are:

at the inlet,

$$p = p_{\text{atm}}, \quad (15)$$

at the flow front,

$$p = p_{\text{atm}} - \Delta p, \quad (16)$$

where p_{atm} is the atmosphere pressure, Δp is the surface tension.

It was seen from their study that the discrepancy between the measured and calculated results was less than that reported by Nguyen et al. [28]. However, the flow front predicted with this model was faster than the measured value. Although no clear explanation was given by the authors for this discrepancy, one possible explanation for the discrepancy is that in the case of the Hele–Shaw model, in order to simplify the calculation, it is assumed that the inertia term can be omitted from the momentum equation and the flow is around a single cylindrical body so that the resulting pattern of streamlines is identical with that in potential flow about the same shape. Therefore, in the Hele–Shaw approximation, although the no-slip boundary condition at the plates $z = \pm b$ (here z is gap-wise coordinate, b is one half of the gap height) can be satisfied, but the no-slip boundary condition at the surface of cylindrical body is not satisfied [37]. Considering that underfill flow in flip-chip package is affected by a set of solder bumps, the geometry is not the same as that in Hele–Shaw model, the surface resistance caused by the solder bumps may have significant influence on the flow. This effect was confirmed by the study reported by Wan [35].

In the study reported by Wan [35], the numerical model was developed based on the Navier–Stokes equation for two-dimensional flow. A time-dependent velocity boundary condition was used in the model to consider the effect of flow resistance at the plates $z = \pm b$ to eliminate the error caused by other two-dimensional models available. The continuity equation and the momentums in this model are, respectively, given by

$$\frac{\partial v_x}{\partial x} + \frac{\partial v_y}{\partial y} = 0, \quad (17)$$

$$\rho \left(\frac{\partial v_x}{\partial t} + v_x \frac{\partial v_x}{\partial x} + v_y \frac{\partial v_x}{\partial y} \right) = -\frac{\partial p}{\partial x} - \left(\frac{\partial \tau_{xx}}{\partial x} + \frac{\partial \tau_{yx}}{\partial y} \right) + \rho g_x, \quad (18)$$

$$\rho \left(\frac{\partial v_y}{\partial t} + v_x \frac{\partial v_y}{\partial x} + v_y \frac{\partial v_y}{\partial y} \right) = -\frac{\partial p}{\partial y} - \left(\frac{\partial \tau_{xy}}{\partial x} + \frac{\partial \tau_{yy}}{\partial y} \right) + \rho g_y, \quad (19)$$

where v_x and v_y are the velocity components in the x and y directions, respectively. p is the pressure, ρ is the fluid

density, and τ is the shear stress, in which the first subscript refers to the plane on which the components of shear stress are acting, and the second indicates the direction of the component on that plane.

The energy equation is given by

$$\rho c_v \left(\frac{\partial T}{\partial t} + v_x \frac{\partial T}{\partial x} + v_y \frac{\partial T}{\partial y} \right) = k \frac{\partial^2 T}{\partial z^2} + \eta \dot{\gamma}^2, \quad (20)$$

where T is the temperature, c_v is the constant volume specific heat, k is the thermal conductivity, and η is the apparent viscosity. $\dot{\gamma}$ is the shear rate and is given by

$$\dot{\gamma} = \sqrt{\left(\frac{\partial v_x}{\partial z} \right)^2 + \left(\frac{\partial v_y}{\partial z} \right)^2}. \quad (21)$$

The non-Newtonian behavior of the typical underfill material used in flip-chip underfill is described with the power-law constitutive equation, which is presented as follows (Macosko, 1994) [38]:

$$\tau_{ij} = m |II_{2D}|^{(n-1)/2} (2D_{ij}), \quad (22)$$

where D is the rate of deformation gradient tensor, τ is the shear stress, and II_{2D} is the second invariant of D . The rate of deformation tensor is given by

$$2D = L + L^T, \quad (23)$$

where L is the velocity gradient tensor and L^T is the transpose of L , which is often written out as the dyad product of the gradient vector (symbol ∇) and the velocity vector, i.e.,

$$\nabla \vec{V} = L^T = \sum_i \sum_j \delta_i \delta_j \frac{\partial v_j}{\partial x_i}, \quad (24)$$

where δ is the unit tensor.

In the inlet, a time-dependent velocity boundary condition was employed instead of the pressure boundary condition to consider the flow resistance exerted by the parallel plates, which is given by

$$u = \frac{nh}{2(n+1)} \left(\frac{\Delta p}{m} \right)^{1/(n+1)} \left(\frac{n+1}{2n+1} \right)^{n/(n+1)} t^{-(1/(n+1))}, \quad (25)$$

where u is the velocity, t is the filling time, h is the gap height, m and n are coefficient and index of power-law viscosity equation, respectively, and Δp is the driving pressure and calculated with the following equation:

$$\Delta p = \frac{2\sigma \cos \theta (W^2 + dW - dh)}{hW(W+d)}, \quad (26)$$

where W is the clearance between two adjacent solder joints, and d is the solder diameter.

The model was implemented using the ANSYS software package (Version 7.0). The finite element method (FEM) was used to discrete the fluid flow equations, and the volume of fluid (VOF) technique was used to track the flow front. The study showed that this model can give good prediction for the underfill flow between two parallel plates both for the filling time and for the flow front distribution.

In the numerical simulation in flip-chip underfill flow, the calculated arithmetic average of the filling time can adequately match the measured results. However, the flow front shape does not match the measured results well, which calls for a further study.

5. Summary and discussion

In this article, the models which have been used to describe the flow properties of underfill are discussed. The models included apply to Newtonian and non-Newtonian behavior with and without the solder bump resistance.

In regard to the analytical models available, the discussion shows that Washburn model only apply to the Newtonian fluid in the underfill flow between two parallel plates driven by capillary action, but it is not applicable to the non-Newtonian fluid. The model improved by Han and Wang by introducing dynamic contact angle to Washburn model to consider the non-Newtonian behavior of underfill material is superior to the original Washburn model for predicting the underfill process in a flip-chip package. However, the predicted filling time still did not match the experimental results well. One of the possible reasons for this discrepancy is this model does not include the effect of the solder bump on the underfill flow as it was developed for the underfill flow between two parallel plates. This effect was confirmed by a model proposed by Wan et al. [33]. The study showed that the prediction using the proposed analytical model with the consideration of solder bump resistance matches the measured filling times better than the predictions using both the Washburn model and the Han–Wang model. This model is better than the Han–Wang model, but it is still basically developed from the Newtonian fluid assumption (Washburn model) and can not match the measured results well. The non-Newtonian viscosity property of the underfill material (i.e., viscosity changes with respect to strain rate) is a major factor to disapprove the model. Therefore, a proper constitutive equation should be employed in our fluid flow analysis to deal with the non-Newtonian behavior of the underfill materials. Wan et al. [34] further developed a new analytical model, in which the power-law constitutive equation is employed for describing the non-Newtonian fluid behavior in the flip-chip packaging. The flow resistance generated by the solder bump in flip-chip package was derived using virtual work principle. Experimental measurements show that this analytical model can give good prediction for the underfill flow in flip-chip packaging.

Regarding the studies for predicting the characteristics of underfill process by numerical method, several typical models were discussed. The numerical model used by Nguyen et al. showed that the predicted motion of the flow front did not match the observed results. One of the possible reasons for the discrepancy is that the authors treated a non-Newtonian encapsulant as Newtonian fluid in their simulation. In the study reported by Han and

Wang [24], the Hele–Shaw approximation was used to describe the underfill flow characteristics for the encapsulant material FP4510. The Hershel–Bulkey constitutive equation was used to describe the non-Newtonian behavior of the underfill material. It was seen from their study that the discrepancy between the measured and calculated results was less than that reported by Nguyen et al. [28]. However, the flow front predicted with this model was faster than the measured value. Although no clear explanation was given by the authors for this discrepancy, one possible explanation for the discrepancy is that in the case of the Hele–Shaw model, in order to simplify the calculation, it is assumed that the inertia term can be omitted from the momentum equation and the flow is around a single cylindrical body so that the resulting pattern of streamlines is identical with that in potential flow about the same shape. Therefore, in the Hele–Shaw approximation, although the no-slip boundary condition at the plates $z = \pm b$ can be satisfied, the no-slip boundary condition at the surface of cylindrical body is not satisfied. Considering that underfill flow in flip-chip package is affected by a set of solder bumps, the geometry is not the same as that in Hele–Shaw model, the surface resistance caused by the solder bumps may have significant influence on the flow.

In the study by Wan [35], the numerical model was developed based on the Navier–Stokes equation for two-dimensional flow. A time-dependent velocity boundary condition was used in the developed model to consider the influence of no-slip boundary condition at the plates $z = \pm b$ on underfill flow. Experimental verification showed that this model can give good prediction for the underfill flow between two parallel plates both for the filling time and for the flow front distribution. In the numerical simulation in flip-chip underfill flow, the calculated arithmetic average of the filling time can adequately match the measured results. However, the flow front shape does not match the measured results well, which calls for a further study.

In all the current studies, when the solder pattern is considered individually, only one pattern of the solder bumps is considered, that is, a full array of regular deployment of the bumps. This particular pattern may not be the best one in terms of the density of connection, though it facilitates the model considerably. There are two questions here: (1) what pattern is the best one in terms of its functionality? and (2) how can the fluids upon any pattern other than the one discussed in the literature be modeled effectively? A further effort on research is certainly needed to answer these questions. Further, the void in the final flip-chip package may likely occur to any process as described before. The question is then how to develop a model to predict the void formation in a particular fluid filling process.

Acknowledgments

The authors would like to thank financial support from the Bureau of Science and Technology of Guangzhou

Municipality and the Bureau of Education of Guangzhou Municipality through research grant. The second and third authors want to thank NSERC for a partial financial support to this research.

References

- [1] C.P. Wong, M.M. Wong, Recent advances in plastic packaging of flip-chip and multichip modules (MCM) of microelectronics, *IEEE Trans. Components Pack. Technol.* 22 (1) (1999) 21–25.
- [2] M.H. Gordon, G. Ni, W.F. Schmidt, R.P. Selvam, A capillary-driven underfill encapsulation process, *Advantaged Pack.* 8 (1999) 34–37.
- [3] J.H. Lau (Ed.), *Flip Chip Technologies*, McGraw-Hill, New York, 1995.
- [4] J.H. Lau, C. Chang, Characteristics and reliability of fast-flow, snap-cure, and reworkable underfills for solder bumped flip chip on low-cost substrates, *IEEE Trans. Electron. Pack. Manuf.* 25 (3) (2002) 231–239.
- [5] J.H. Lau, C. Chang, Characterization of underfill materials for functional solder bumped flip chips on board applications, *IEEE Trans. Components Pack. Technol.* 22 (1) (1999) 111–119.
- [6] A. Gertach, H. Lambach, D. Seidel, Propagation of adhesives in joints during capillary adhesive bonding of micro-components, *Microsyst. Technol.* 6 (1999) 19–22.
- [7] D.R. Gamota, C.M. Melton, Advanced encapsulant materials systems for flip chip on board assemblies: I. encapsulant materials with improved manufacturing properties: II. Materials to integrate the reflow and underfilling processes, in: *IEEE/CPMT International Electronics Manufacturing Technology Symposium*, Austin, TX, 1996, pp. 1–9.
- [8] J. Giesler, G. O'Malley, M. Williams, S. Machuga, Flip chip on board connection technology: process characterization and reliability, *IEEE Trans. Components, Pack. Manuf. Technol.* 17 (3) (1994) 256–263.
- [9] D. Suryanarayana, T.Y. Wu, J.A. Varcoe, Encapsulants used in flip chip packages, *IEEE Transactions on Components and Hybrids Manufacture Technology* 16 (8) (1993) 858–862.
- [10] D. Suryanarayana, R. Hsiao, T.P. Gall, J.M. McCreary, Enhancement of flip chip fatigue life by encapsulation, *IEEE Trans. Component, Hybr.* 14 (1) (1991) 218–223.
- [11] S.C. Machuga, S.E. Lindsey, K.D. Moore, A.F. Skipor, Encapsulation of flip chip structures, *Electronics Manufacturing Technology Symposium*, 1992, Thirteenth IEEE/CHMT International, 28–30 September 1992, pp. 53–58.
- [12] C.P. Wong, D. Baldwin, No-flow underfill for flip-chip packages, *US Patent Disclosure*, April 1996.
- [13] Z. Zhang, C.P. Wong, Recent advances in flip-chip underfill: materials, process, and reliability, *IEEE Trans. Adv. Pack.* 27 (3) (2004) 515–524.
- [14] Y.K. Shen, T.W. Ye, S.L. Chen, C.H. Yin, W.D. Song, Study on mold flow analysis of flip chip package, *Int. Commun. Heat Mass Transfer* 28 (2001) 943–952.
- [15] S. Han, K.K. Wang, Study on the pressurized underfill encapsulation of flip-chips, *IEEE Trans. Components, Pack. Manuf. Technol.* B 20 (4) (1997) 434–442.
- [16] K. Chai, E. Wu, R. Hsieh, J.Y. Tong, Challenge of flip chip encapsulation technologies, in: *Proceedings of SPIE—The International Society for Optical Engineering*, Denver, CO, USA, 4931, 2002 pp.733–737.
- [17] K. Chai, E. Wu, The underfill processing technologies for flip chip packaging, in: *First International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics: Incorporating POLY, PEP and Adhesives in Electronics*, Potsdam, Germany, 2001, pp. 119–123.
- [18] L.P. Rector, S. Gong, K. Gaffney, 2001, On the performance of epoxy molding compounds for flip-chip underfill transfer molding

- encapsulation, in: Proceedings of the 51st Electronic Components Technology Conference, Orlando, FL, pp. 293–297.
- [19] J. Wang, Flow time measurement for underfills in flip-chip packaging, *IEEE Trans. Components Pack. Technol.* 28 (2) (2005) 366–370.
- [20] J. Wang, Underfill of flip-chip on organic substrate: viscosity, Surface Contact Angle Microelectron. Reliab. 42 (2002) 293–299.
- [21] C.Y. Huang, The investigation of the capillary flow of underfill materials, *Microelectron. Int.* 19 (1) (2002) 23–29.
- [22] Y. Guo, G.L. Lehmann, T. Driscoll, E.J. Cotts, A Model of the underfill flow process: particle distribution effects, in: Proceedings of the 1999 49th Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 1999, pp. 71–76.
- [23] N.W. Pascarella, D.F. Baldin, Compression flow modeling of underfill encapsulation for low cost Flip-Chip Assembly, *IEEE Trans. Components, Pack. Manuf. Technol. C* 21 (4) (1998) 325–335.
- [24] S. Han, K.K. Wang, Analysis of the flow of encapsulant during underfill encapsulation of flip-chips, *IEEE Trans. Components, Pack. Manuf. Technol. B* 20 (4) (1997) 424–433.
- [25] M.K. Schwiebert, W.H. Leong, Underfill flow as viscous flow between parallel plates driven by capillary action, *IEEE Trans. Components, Pack. Manuf. Technol. C* 19 (12) (1996) 133–137.
- [26] E.W. Washburn, The dynamics of capillary flow, *Phys. Rev.* 17 (1921) 273–283.
- [27] P. Fine, B. Cobb, L. Nguyen, Flip-chip underfill flow characteristics and prediction, *IEEE Trans. Components Pack. Technol.* 23 (3) (2000) 420–427.
- [28] L. Nguyen, C. Quentin, P. Fine, B. Cobb, S. Bayyuk, H. Yang, S.A. Bidstrup-Allen, Underfill of Flip-chip on laminate: simulation and validation, *IEEE Trans. Components Pack. Technol.* 22 (2) (1999) 168–176.
- [29] G.L. Lehmann, T. Driscoll, N.R. Gydosh, P.C. Li, E.J. Cotts, Underflow process for direct-chip-attachment packaging, *IEEE Trans. Components, Pack. Manuf. Technol. A* 21 (2) (1998) 266–274.
- [30] G. Lehmann, A. Maria, Pin-Chou Lee, E.J. Cotts, Modeling the underfill flow process, in: Proceedings of the Technical Program, Conference on Surface Mount Technology, San Jose, CA, 1997, pp. 340–350.
- [31] H. Schonhorn, H. Frisch, T.K. Kwei, Kinetics of wetting of surfaces by polymer melts, *J. Appl. Phys.* 37 (1966) 4967–4973.
- [32] S. Newman, Kinetics of wetting of surfaces by polymer: capillary flow, *J. Colloid Interface Sci.* 26 (1968) 209–213.
- [33] J.W. Wan, W.J. Zhang, D.J. Bergstrom, Influence of transient flow and solder bump resistance on underfill process, *Microelectron. J.* 36 (8) (2005).
- [34] J.W. Wan, W.J. Zhang, D.J. Bergstrom, An analytical model for predicting the underfill flow characteristics in flip-chip encapsulation, *IEEE Trans. Adv. Pack.* 28 (3) (2005).
- [35] J.W. Wan, Analysis and modeling of underfill flow driven by capillary action in flip-chip packaging, Ph.D. Dissertation, University of Saskatchewan, Saskatoon, SK, Canada, 2005.
- [36] Wen-Bin Young, Wen-Lin Yang, Underfill viscous flow between parallel plates and solder bumps, *IEEE Trans. Components Pack. Technol.* 25 (4) (2002) 695–700.
- [37] H. Schlichting, *Boundary-layer Theory*, McGraw-Hill, New York, Toronto, 1979.
- [38] C.W. Macosko, *Rheology: Principles, Measurements, and Applications*, VCH Publishers, Inc., New York, 1994.